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# Modeling and Simulation of Low Power 1-bit CMOS Full Adder Cells

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## ABSTRACT

*The optimization of virtual supply network plays an important role in MTCMOS low-power design..In modern high performance systems-on-chips (SoCs), more than 40% of the total active mode energy can be dissipated due to the leakage currents. With more transistors integrated on-die, leakage currents will soon dominate the total energy consumption of high performance SoCs. Furthermore, leakage current is the only source of energy consumption in an idle circuit. The battery-powered portable systems such as cell phones and laptop computers tend to have long standby modes. Reducing the leakage energy consumption of the portable systems during these long idle periods is crucial for a longer battery lifetime. As the VLSI technology and supply voltage continue scaling down, leakage power has become more and more significant in the power dissipation of today's CMOS circuits. This paper proposed a design technique to reduce leakage current in one bit full adder cell. This technique uses transistor stack effect to decrease the leakage current and leakage power also. This work analyzed the leakage current and leakage power of a full adder cell by applying the proposed technique. The delay of sum and carry outputs are also analyzed for the stack technique. The supply voltage is varied from 0.5 volt to 0.8 volt. We have reduced leakage current upto 38% and leakage power upto 68%.*

***Keywords:—****Low Power, Leakage Current, Full Adder, CMOS Process Technology, transistor stacking.*

## I. INTRODUCTION

The extensive development in the field of portable systems and cellular networks has intensified the research efforts in low power microelectronics. The low-power design has become a major design consideration. The design criterion of a full adder cell is usually multi-fold. Transistor count is, of course, a primary concern which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit (ALU). The limited power supply capability of present battery technology has made power consumption an important figure in portable devices [1]. The speed of the design is limited by size of the transistors, parasitic capacitance and delay in the critical path. The driving capability of a full adder is very important, because, full adders are mostly used in cascade configuration, where the output of one provides the input for other. If the full adders lack driving capability then it requires additional buffer, which consequently increases the power dissipation. In the last decade, the full adder has gone through substantial improvement in power consumption, speed and size, but at the cost of

weak driving capability and reduced voltage swing. However, reduced voltage swing has the advantage of lower power consumption [2].There is no ideal full adder cell that can be used in all types of applications. Hence novel architectures such as CMOS, Transmission Gate (TG), Pass-Transistor Logic (PTL), Complementary Pass-transistor Logic (CPL) [3] and Gate Diffusion Input (GDI) are proposed to meet the requirements. Each design style has its own share of advantages and disadvantages. Moore's law as we know will no longer exist in a near future, and one can already see the phenomenon of reduction of clock frequency due to excessive power dissipation. The reason is very simple, physical limits of silicon, since it is not possible to shrink atoms. Therefore, new technologies that will completely or partially replace silicon are arising. According to the ITRS roadmap[1], these technologies have a high level of density and are slow, or the opposite: can achieve high speeds but with a huge area overhead even when comparing to future CMOS technology. Hence, traditional systems will suffer from the same problems that embedded systems suffer today: the necessity of increasing performance with severe area and power constraints. Additionally, traditional high performance architectures as the diffused superscalar machine are also achieving their limits, and recent increases in performance occurred mainly thanks to boosts in clock frequency. As an example, the clock frequency of Intel's Pentium 4 processor only increased from 3.06 to 3.2 GHz between 2002 and 2003[2]. This way, the frequency increase rate reduction, together with the foreseen slow technologies are new architectural challenges to be dealt with. In most VLSI applications, arithmetic operations play an important role. Commonly used operations are addition, subtraction, multiplication and accumulation, and the 1- bit Full Adder (FA) cell is the building block for most implementations of these operations. Obviously, enhancing the building block performance is critical for enhancing overall system performance [3]-[6]. The vast use of this operation in arithmetic functions attracts many researchers to this field. In recent years several variants of different logic styles have been proposed to implement 1-bit adder cells [6]-[23]. They commonly aimed to reduce power consumption and increase speed. With the increasing demand for battery-operated portable applications such as cell phones, PDAs and laptop computers, as well as low-intensity applications such as distributed sensor networks, the need for power sensitive design has grown significantly. It has been shown that reducing the supply voltage is the most direct means of reducing dissipated power [5], [6], and operating CMOS devices in the subthreshold region is considered to be the most energy-efficient solution for low-performance applications [5].

Designing low-power VLSI systems has become an important performance aim because of the fast growing technology in mobile computation and communication field [24], [25]. There is one basic approach to reduce power consumption of circuits in scaled technologies. One approach is reducing the dynamic power consumption during the active mode operation of the device and the other is the reduction of leakage current during the standby mode[26]. The power consumption of a CMOS digital circuit can be expressed as in equation (1) and equation (2).

$$P = P_{dynamic} + P_{short} + P_{leakage} \quad \text{.....(1)}$$

$$P = f.C.Vdd^2 + \alpha\, f.I_{short}.Vdd + I_{leak}.\, Vdd \quad \text{.....(2)}$$

Where f is the clock frequency, C is the average switched capacitance per clock cycle, Vdd is the supply voltage, $I_{short}$ is the short circuit current and $I_{leak}$ is the off current. Supply voltage reduction is a widely accepted methodology for reducing dynamic power, but it has an adverse effect on circuit performance. To maintain high performance, the threshold voltage $V_t$ must also be scaled down that causes an exponential increase in the sub-

threshold leakage[27]. Static power dissipation is the power dissipated by the circuit when it is in sleep mode or standby mode. Average leakage power is given by equation (3).

$$Pleak = \frac{1}{T \int Ileak * Vdd} \quad \text{.....(3)}$$

Where $I_{leak}$ is the leakage current that flows in a transistor when it is in off state. This static power dominates dynamic power especially in deep sub micron circuits and also in circuits that remains in idle mode for a long time like cell phones.

The adder is one of the most critical components of a processor, as it is used in the arithmetic logic unit (ALU), in the floating-point unit, and for address generation in case of cache or memory access. A one bit full adder cell is the most important and basic block of an arithmetic unit of a system. Obviously, improving its performance and decreasing its power directly leads to low power and high performance of the whole system. Therefore in this paper the focus is on the reduction of leakage current consumption of 28 transistor (28T) full adder cell which is very high in sub-micron technology. The rest of the paper is organized as follows. Section 2 presents the operation of 1 bit full adder section 3 presents proposed leakage reduction techniques. Section 4 presents the simulation results of the full adder with and without the leakage reduction technique and section 5 gives the conclusion.

## II. Working of 1 Bit Full Adder

A Full Adder (FA) is a logical circuit that performs an addition operation on three binary digits. The full adder produces a sum and a carry value, which are both binary digits. The logical diagram of full adder is shown in figure 1.

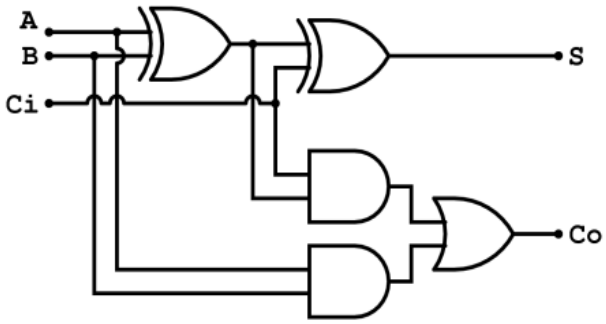


*Figure 1 : Logic Diagram of full adder*

A FA adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as *A*, *B*, and *C*i here *A*, *B* are the operands, and *C*i is a bit carried in (in theory from a past addition by [32]). The circuit produces a two-bit output sum typically represented by the signals *C*o (Carry) and *S* (Sum). The Boolean equation and truth table are shown bellow.

S= A XOR B XOR C…….(4)
C0= (A AND B) OR (B AND Ci) OR (Ci AND A)……..(5)

**Table 1: Truth Table for Full Adder**

| A | B | Ci | Sum (S) | Carry (C0) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

A FA can be constructed by cascading of two HA (Half Adder). The *A* and *B* are connected to the input of first HA and the sum of first HA is connected as one input along with Ci to second HA and it give SUM output. The logical OR of first and second HAs carry

outputs a gives CARRY output of FA shown in [33]. A schematic of one bit full adder is shown in figure 2. Figure 3 shows the functionality of full adder.

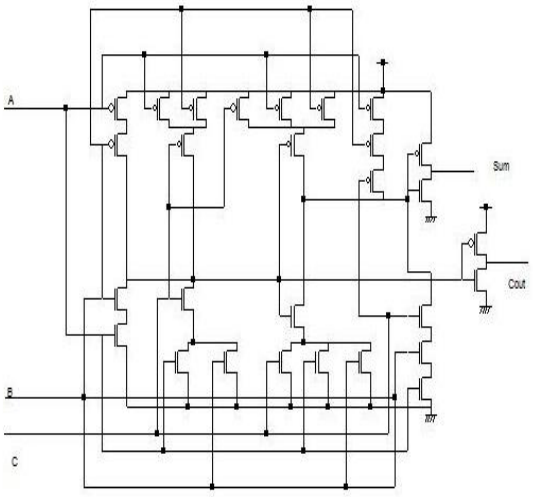


*Figure 2: Schematic of 28 Transistor Full Adder*

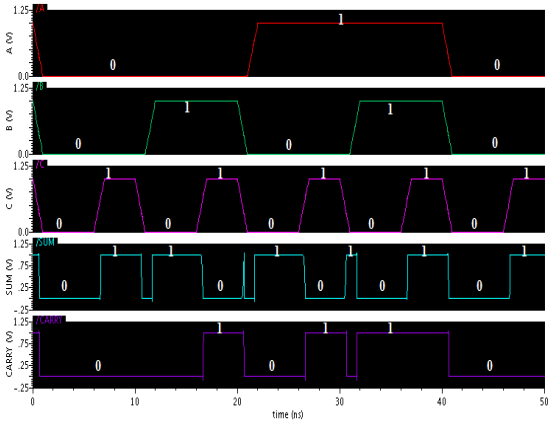


*Figure 3: Functionality of Full Adder*

## III. Leakage Control Using Transistor Stacking

The leakage current flowing through a stack of series connected transistors reduces when more than one transistor of the stack is turned OFF. This effect is known as the "Stacking Effect". When two or more transistors that are switched OFF are stacked on top of each other as shown in figure 4 (A), then they dissipate less leakage power than a single transistor that is turned OFF [Refer Figure 4 (B)]. This is because each transistor in the stack induces a slight reverse bias between the gate and source of the transistor right below it, and this increases the threshold voltage of the bottom transistor making it more resistant to leakage. Therefore in Figure 4 (A) transistor T2 leaks less current than transistor T1 and T3 leaks less than T2. Hence the total leakage current through the transistors T1,T2 and T3 is decreased as it flows from Vdd to ground node. So $I_{leak1}$ is less than $I_{leak2}$ [29]. If natural stacking of transistors do not exist in a circuit, then to utilize the stacking effect a single transistor of width W is replaced by two transistors each of width W/2 [30] as shown in Figure 4 (C).

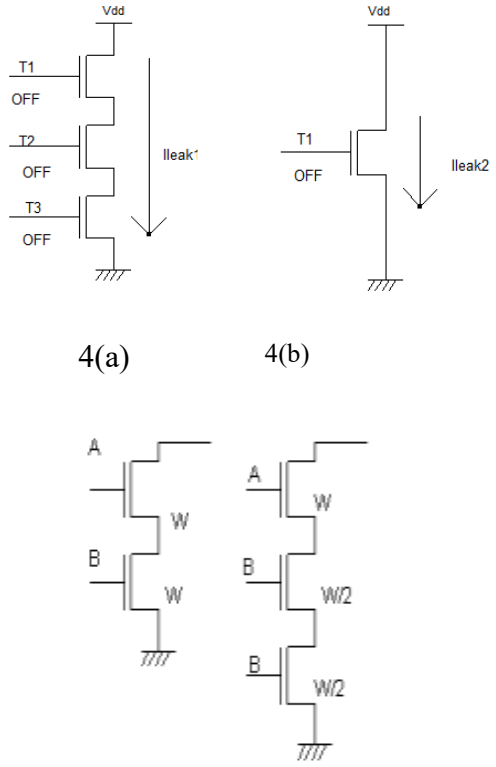


*Figure 4: Transistor Stacking Effect*

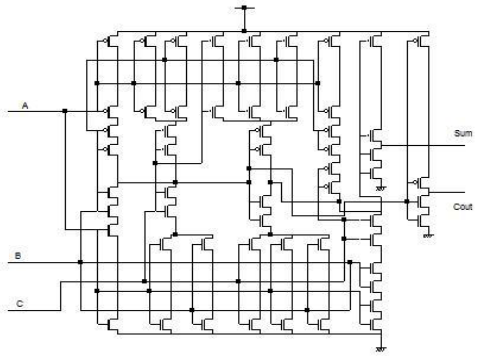


*Figure 5: Circuit of a 28 transistor Full Adder with stack*

## 4. Simulation Result

In this paper, a 28T full adder cell is implemented in 45 nm technology. Initially the leakage current of the above circuit is computed without any reduction technique (Base case). Then the proposed methods transistor stacking (Stack) is applied to the circuits. Figure 2 and Figure 5 shows the circuit of a 28T full adder cell and full adder with stack respectively. The simulations are performed on Cadence Virtuoso tool in 45 nm CMOS process technology at a temperature of 27º C by varying the supply voltage Vdd from 0.5 volt to 0.8 volt. The simulation results are shown in figure 6 and figure 7. The result shows that with the proposed method stack technique, the leakage current decreases at all supply voltages ranging from 0.5 volt to 0.8 volt and the reduction is more with the stacking method.

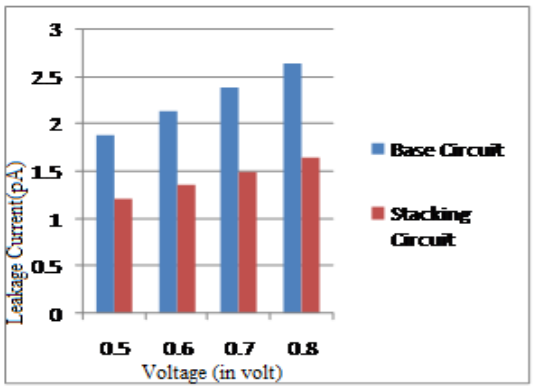


*Figure 6: Comparison of Leakage Current between Base Circuit and Stacked Circuit*

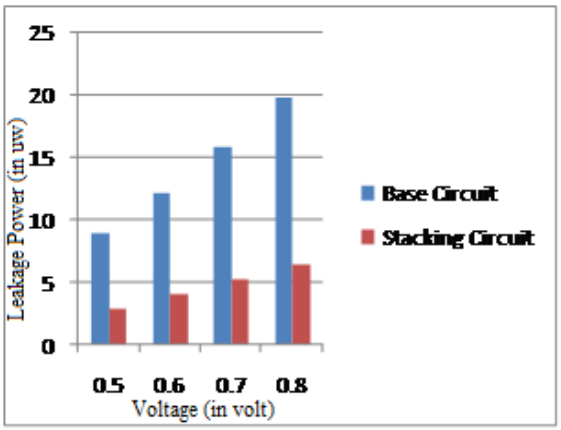


*Figure 7: Comparison of Leakage Power between Base Circuit and Stacked Circuit*

## 5. Conclusion

It can be seen that the highest speed of operation i.e. Minimum delay is achieved by circuit with low threshold MOSFET in P-net and N-net. However, it has moderate power consumption and excessively high leakage power consumption. Again, the speed of operation is lowest i.e. Maximum delay is achieved by the circuit with high threshold MOSFET in P-net and N-net. Moreover, highest average power consumption is there. However, it has very low leakage power consumption. Finally, the speed of operation is Modest i.e. intermediate delay is achieved by the circuit with high and low threshold MOSFET in Nnet and P-net respectively. Moreover, it has lowest average power consumption and very low leakage power consumption. So, it can be successfully concluded that considering all design constraints, circuit with high and low threshold MOSFET in N-net and P-net respectively. In this work the analysis of leakage current of a 28T full adder cell is carried out in 45nm CMOS process technology at different supply voltages using stacking reduction techniques. The leakage current decreases with the proposed technique and the reduction is more with stacking. So a low leakage adder for use in the arithmetic unit of a processor can be designed using the proposed methods.

## VI. ACKNOWLEDGEMENT

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