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Optimized Multi Level Logic for Digital System

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ABSTRACT

A Multi Logic Memory cell have various logic between one and zero that's why fuzzy logic is also known as multiple-logic level, when the paper work was in plan originally plan was do something in Fuzzy Electronics. Lots of fuzzy systems is been developed already but from observing fuzzy flip-flops working the idea comes for the proposed work. Paper work propose designs of a new fuzzy memory cell (flip-flop) for four logic levels which can hold Logic 0, Logic 1, Logic 2 and Logic 3 total four fix logic .though fuzzy logic deals with approximate logic rather than fix proposed work has fix logic and it is the big difference between proposed work and fuzzy based memory cell. Proposed work also has design an Interfacing module between fuzzy memory with Digital) systems, just for make proposed four logic flip-flop compatible with existing binary logic based digital system application for proposed design that one can reduce the no. of wires required when to establish parallel interface with memory and also one can increase the speed or throughput of simple serial data transfer.

Keywords:— *flip flop, memory cell, logic gate, tanner*

I. INTRODUCTION

Fuzzy Electronics logic also known as many-valued logic it works with theory that is approximate than fixed and rigid. Compare with traditional logic theory, where binary sets have two valued logic, one or zero, fuzzy logic variables may have a value that lies in degree between 0 and 1.

Binary logic system: Digital electronics circuits that have exactly two possible state either 0 or 1. There are some very simple logic gates that can compute almost everything. Also a different combination of logic gates gives us the Flip flops which can store of the data. '0' and '1' are logical concept of two possible conditions (true and false), for actual presentation of these, there are some standard logic families like ECL, TTL, CMOS etc.

Table 1 : TTL Input/output high ('1') and low ('0')

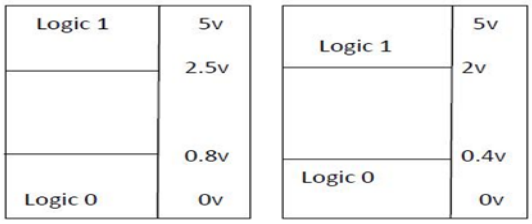

Table 1 shows the how the logic '1' and '0' exist in the actually, it is in the form of some voltage ranges. **Multi Level Logic:** Fuzzy logic can have many logic between true and false, here paper work proposed a type of Fuzzy logic which has four logic levels Logic '0', Logic '1', Logic '2' and Logic '3' as showed in Figure 2.

Table 2: The voltage range of our proposed multi level logic

Voltage range IN/Out	Multi level logic
0 to 1v	Logic '0'
1 to 3v	Logic '1'
3to 5v	Logic '2'
5 to 6v	Logic '3'

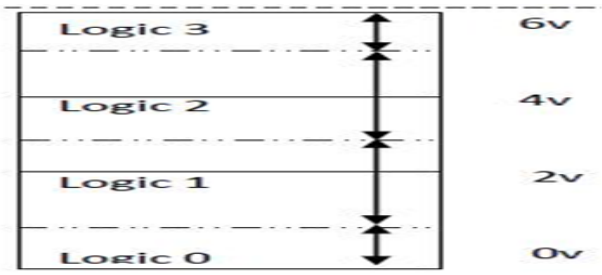

Figure 1: Multi Level Logic

Binary Logic V/S Multi Level Logic: Tables number 2, 3, 4 and 5 shown below to observe the difference between basic Digital binary Logic Gates and Multi level Logic Gate.

Table 3: Binary AND Gate

Binary AND logic		
Input		**Output**
0	0	0
0	1	0
1	0	0
1	1	1

Table 4: Binary OR GATE

Binary OR logic		
Input		**Output**
0	0	0
0	1	1
1	0	1
1	1	1

Table 5: Multi Level Fuzzy AND Gate

Four logic AND		
Input's		**Output**
0	0	0
0	1	0
0	2	0
0	3	0
1	0	0
1	1	1
1	2	1
1	3	1
2	0	0
2	1	1
2	2	2
2	3	2
3	0	0
3	1	1
3	2	2
3	3	3

As from new logic gate, one can also have multi logic level Flip Flop (Cell). A normal binary flip flop can hold only two logic level (i.e. '1' or '0') however proposed Multi Level FF can hold four logic levels. As known a register is a configuration of Flip flops and a configuration of registers is memory (Static RAM), for storing any decimal number range between 0 to 255. It is required to configure 8 Flip-flops in one register as shown in the figure 2, and it used by memory for store 1 byte

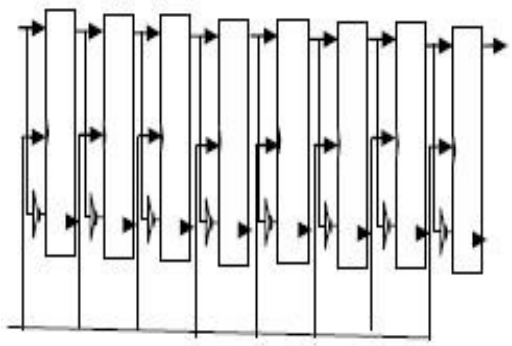

Figure 2: Binary FF based Register for storage of decimal range 0 to 255

Table 6: Multi level Logic OR Gate

Four logic OR		
Input's		Output
0	0	0
0	1	1
0	2	2
0	3	3
1	0	1
1	1	1
1	1	1
1	2	2
1	3	3
2	0	1
2	1	1
2	2	2
2	3	3
3	0	3
3	1	3
3	2	3
3	3	3

But if concerns about Multi Level Register for storing the decimal number ranges between 0 to 255. There need of Multi Level proposed flip-flops only as shown in figure 3. Proposed memory cell will use to store 4 Multi Level logic (0 or 1 or 2 or 3).

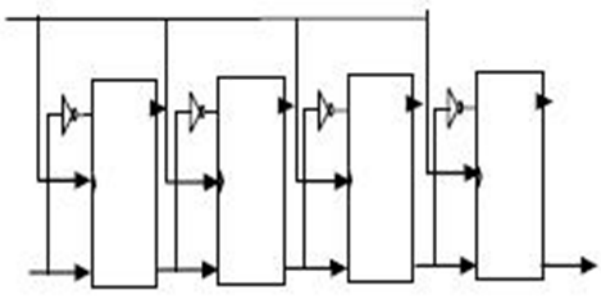

Figure 3: Multi Level Fuzzy Register for storage of decimal range 0 to 255

II. Proposed Methodology

We have planned to implement our design as per VLSI design flow and to design an efficient multi-value logic for the application where high speed required and less power.

In logic, a many-valued logic (also multi- or multiple-valued logic) is a propositional calculus in which there are more than two truth values. Traditionally, in Aristotle's logical calculus, there were only two possible values (i.e., "true" and "false") for any proposition. Classical two-valued logic may be extended to n-valued logic for n greater than 2. Those most popular in the literature are three-valued (e.g., Łukasiewicz's and Kleene's, which accept the values "true", "false", and "unknown"), the finite-valued (finitely-many valued) with more than three values, and the infinite -valued (infinitely-many valued), such as fuzzy logic and probability logicmulti-logic should be simple as binary logic and it should perform computations easily like binary logic, actually binary logic can perform computation easily because it used Boolean algebra and binary logic gates, there for to make multi-value logic can perform simplified computation we also need to design multi logic Gates.

As we know binary TTL logic has two logic '0' and '1' and the voltage range for binary '0' is from 0 v to 0.8 v and for binary '1' it 2.4v to 5v for input and for output voltage range for binary '0' is from 0 v to 0.4 v and for binary '1' it 2v to 5v, As we can see here the noise margin is of 0.4 v, when we go for the multi-value logic then choosing number of levels becomes a tedious job because if we increase the maximum voltage (5v) then the power requirements increases and if we increase the logic levels the good noise margin cannot be achieved. Hence we need to choose number of binary levels which will have efficient noise

margin and voltage range which does not increase power requirement of system. Proposed works is the solution for that problem which use a new flip flop of 4 logic levels.

Guaranteed if the premises are jointly true, because the application of valid steps preserves the property. However, that property doesn't have to be that of "truth"; instead, it can be some other concept.

Most of the existing digital systems are designed for binary logic and perform binary computations and multi-value logic used multiple logic for computation in digital systems hence we suppose to design some system which interface with existing binary based systems.

Multi logic levels

As we know binary TTL logic has two logic '0' and '1' and the voltage range for binary '0' is from 0 v to 0.8 v and for binary '1' it 2.4v to 5v for input and for output voltage range for binary '0' is from 0 v to 0.4 v and for binary '1' it 2v to 5v, As we can see here the noise margin is of 0.4 v, when we go for the multi-value logic then choosing number of levels becomes a tedious job because if we increase the maximum voltage (5v) then the power requirements increases and if we increase the logic levels the good noise margin cannot be achieved. Hence we need to choose number of binary levels which will have efficient noise margin and voltage range which does not increase power requirement of system.

To solve the problem above we have choose to design 4 logic levels between 0v to 6v .

Table 7: 4 logic levels voltage range

Voltage Range in/out	Multilevel logic
0V to 1V	Logic _0'
1V to 3V	Logic _1'
3V to 5V	Logic _2'
5V to 6V	Logic _3'

Binary to multi-logic convertor: Another problem is that most of the existing digital systems are designed for binary logic and perform binary computations and multi-value logic used multiple logic for computation in digital systems hence we suppose to design some system which interface with existing binary based systems.

Figure shown below is the design which I proposed for the solution of above problem. Here I designed two major modules first an encoder second a voltage translator.

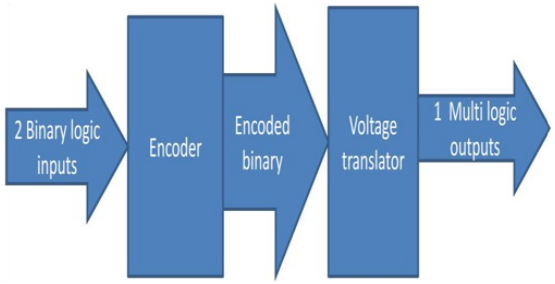

Figure 4: Block diagram of proposed binary to multi-logic convertor

Table 8 : Binary to multi-logic convertor truth table

Binary INPUT'S		Multi logic OUTPUT
0 (0-0.8 V)	0(0-0.8 V)	0 (0-1 V)
0(0-0.8 V)	1(3-2.5V)	1(1-3V)
1(3-2.5V)	0(0-0.8 V)	2(3-5V)
1(3-2.5V)	1(3-2.5V)	3(5-6V)

III. Tools and Platform Use

Xilinx ISE Software: This EDA tool supports the Integrated Software Environment (ISE). It also generate bit file (netlist file) so it can implement RTL code design on FPGA.

Tanner EDA: Tanner EDA provides a full line of software solutions for full custom design and also catalyzes innovation for the design, schematic and verification of analog and mixed signal (A/MS) integrated circuits (ICs).

IV. Results

Figure 5 shown below is the schematic design S-edit of proposed multi level logic AND gate designed by Tanner T-spice pro v6.02

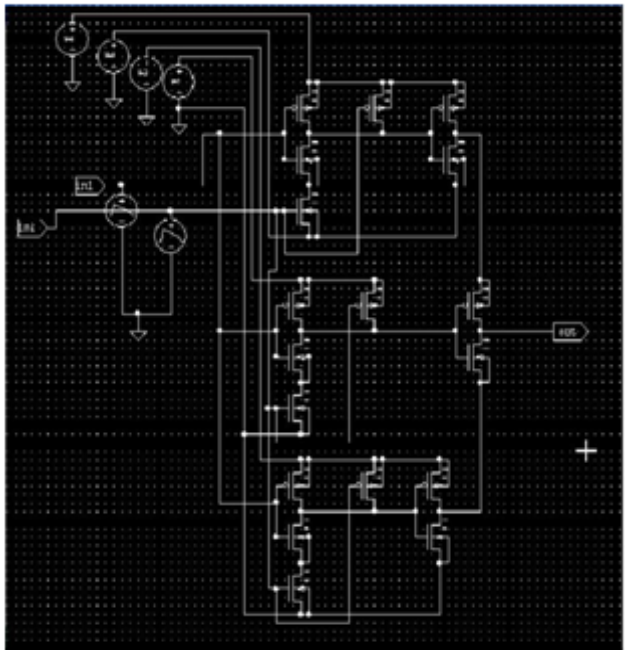

Figure 5: Multi level AND logic gate

Figure 6 is the simulation result generated using Tanner tool for the schematic shown in the figure 4.

Figure 7 is the S-edit schematic design of multi level logic OR gate designed by Tanner T-spice pro v6.02

Figure 8 is the simulation result generated using Tanner tool for the schematic shown in the figure 5.

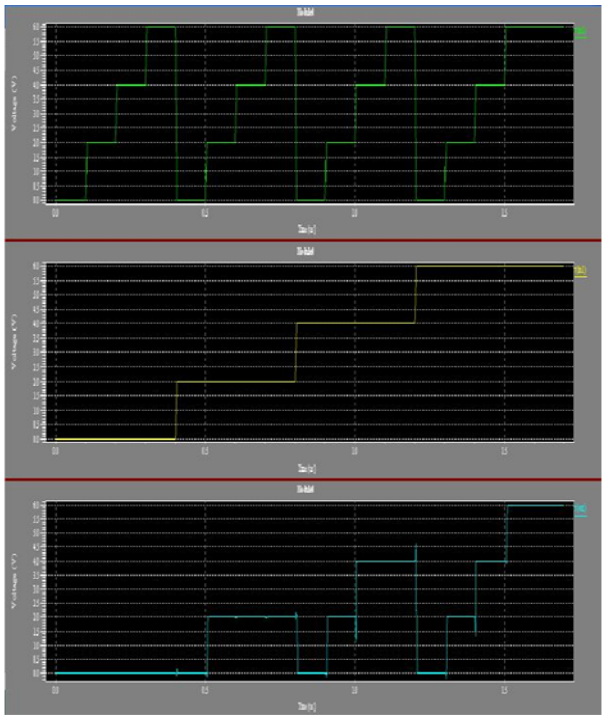

Figure 6: Simulation of Multi level AND Logic

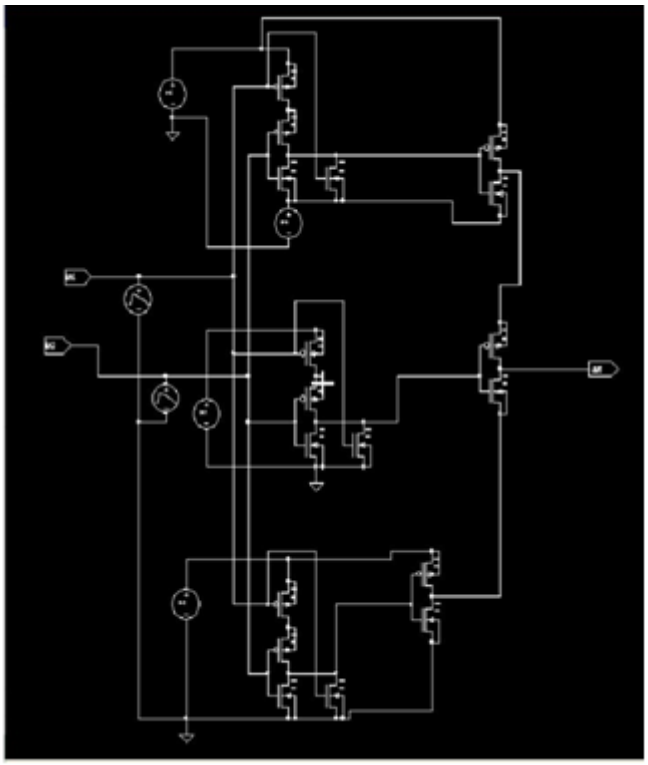

Figure 7: Multi Level OR Logic gate

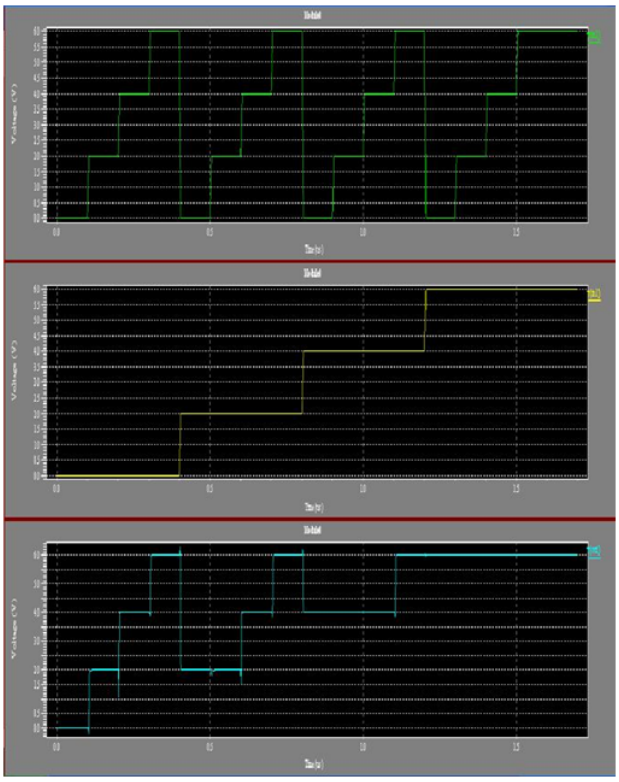

Figure 8: Simulation of multi level OR Gate

Results are been verified correctly and observed as was expected but there is only one problem of noise margin this logic proposed design provides noise margin of only 0.7 v.

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V. CONCLUSION

Our work concentrated on digital approaches, which results in multi valued logic gates. Proposed work slightly modified already done designs of the many valued AND gate and OR gate in an try to test them using digital components or using of the-shelf discrete components, the observed test results do not generates ideal outputs. So, future research may focus on the improvement on the realization of multi valued logic gates also the improvement on the realization of fix multi-valued logic gates. The proposed design observed results are verified in local environment with ideal transistor parameters and found good and expectable but still more precision can be done in future. The power consumption of the proposed design is 3.95 mW which is less as compare to previous designs and transient time is 157ms which give a good throughput for the proposed flipflop.

REFERENCES:

[1] Baturone, I; Barriga, A; Sanchez-Solano, S; Lopez,

[2] D.R; "Microelectronic Design of Fuzzy Logic-Based Systems", CRC Press, ISBN 0-8493-0091-6,.

[3] New Components for Building Fuzzy Logic Circuits,Ben Choi and Kunal Tipnis,Computer Science and Electrical Engineering, Louisiana Tech University, LA 71272, USA

[4] Marinos, P; "Fuzzy logic and its application to switching systems" IEEE Transactions on Computing, vol. C-18, no.4, p 343-348, Apr 1969.

[5] Leslaw, G.; Kluska, J.; "Family of fuzzy J-K flip-flops based on bounded product, bounded sum and complementation" IEEE Transactions on Systems, Man, and Cybernetics, Part B: Cybernetics, vol. 28, n 6, Dec,1998, p 861-868.

[6] Mendel, J.M.; "Fuzzy Logic Systems for Engineering: A Tutorial" Proceedings of IEEE, vol. 83, No.3, March 1995.

[7] Miki, T; Yamakawa, T; "Fuzzy Inference on an Analog Fuzzy Chip," IEEE Micro, pp. 8-18, 1995.

[8] McLeod, D.; Pedrycz, W.; Diamond,

J.; "Fuzzy JK flipflops as computational structures: design and implementation" IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 41, n 3, Mar, 1994, p 215-226.

[9] Simulink; "Simulink: Simulation and Model Based Design" version 6, The Mathworks, 2005.

[10] Zadeh, L.A.; "Fuzzy Logic = Computing with words" IEEE Transactions on Fuzzy Systems, vol.4, p 103-11, 1996.

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