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Calculation of Power and Delay of a 4:1 Multiplexer using Low Power Techniques

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ABSTRACT

*The Low power has become an important issue in today's consumer Electronics. Any combinational circuit can be represented as a multiple inputs with single output. Multiplexer is a primary cell for every digital circuit. In this paper, I design and simulate 4*1 multiplexer using conventional and GDI, FINFET, LEAP techniques. I have also done comparatively study with conventional CMOS Design on the principle of speed, transistor count and power consumption. The GDI cell consists of only two transistors PMOS and NMOS for implementation of wide range of logic circuits. VDD supply of PMOS is not connected in GDI cell and on the other hand NMOS is not linked to GND. This characteristic makes the GDI cell technique effective by using two additional input pins which are very useful to make the design more compatible in terms of no input increasing in the digital circuits. In FINFET, Two transistor of same kind connected with their source and drain terminals attached together. In LEAP logic, PMOS is used as a feedback to store degraded logic, 1" from output of NMOS pass transistor which is called a level restorer. I reduce transistor count, delay and power with the help of GDI technique. Cadence tool is used for simulation of results on 45nm technology.*

Keywords:— *CMOS, GDI, FINFET, LEAP, power dissipation, speed, transistor count.*

I. INTRODUCTION

One of the critical problems in today era is low power consumption within the system. SOC design completely changed for low-power design techniques and technologies in high-speed interface applications square measure developed and conjointly useful within the sensible designs[1].

There are several ways in which the square the measure is broadly used for decreasing the facility dissipation in circuitry by dropping the load capacitances, change activities and offer voltage. These ways solely try and minimize the facility dissipation. However, still maximum amount of the energy down from DC power offer is totally dissipated within the circuit. Other substitute technique for decreasing power consumption is to use the adiabatic logic design. The adiabatic logic circuits will scale back the capability dissipation up-to a massive amount by utilizing the alternating current power offer for the consumption of the energy that holds on into the load of capacitance instead of dissipating the energy with unnecessary heat contained by the circuit [2]. The repetitive shrink in dimension of CMOS circuits and due to this chip density is increases and operations of frequency have made power consumption a

considerable concern in VLSI design [3]. The foremost reason for the selection of proper combinational logic circuit is for the involvements of parameters like short-circuit current, switching capacitance of the circuit and transition action. Switch logic are being realized using multiplexer logic. It is the primary building cell of every logic circuit. Switch logics are being designed using combinational reference block and not by the logic gates. It is used for the designing of logic devices, central processing units and various programmable logic designs [4]. Multiplexers are the type of digital devices which have various inputs and only single output. The output is nothing but is merely either of the inputs and the selection of the inputs is determined by the combination of the select lines. It works on Parallel Input Serial Output (PISO) principle. If we have an m-to-1 MUX, where m=2n, then we would have to use „n" select lines for selecting the „m" inputs consequently. Thus, different types of MUX can be made like 2:1, 4:1, 8:1, 16:1, 32:1 etc., by choosing the 'n' number of select lines [5].

II. 4:1 MULTIPLEXER

Multiplexer is a circuit in which n select lines select one of 2^n input lines and selected line goes to output. Multiplexer is a fundamental component in designing control systems and dynamic circuits.

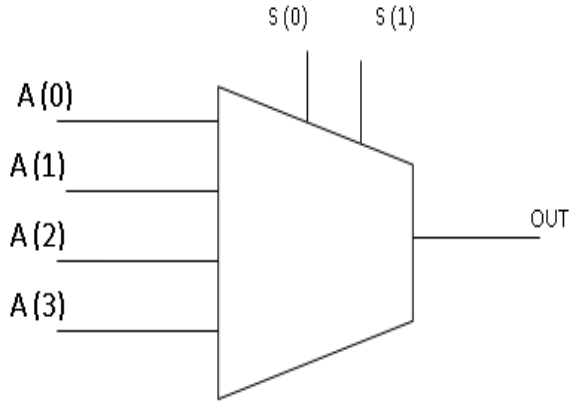

Figure (1) Conventional 4:1 multiplexer

Multiplexer has two select lines C(0) and C(1) which are used for selection and four sets of inputs A(0),A(1), A (2), A(3). Output of multiplexer is in a one bit Y, which is one of the 2^n input lines.

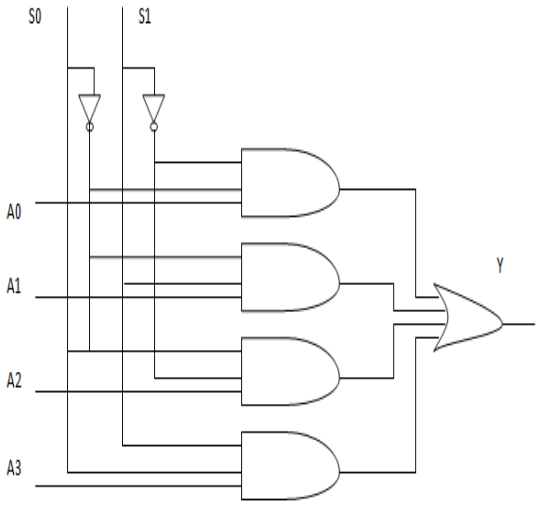

Figure 2 (a) Gate Implementation of 4:1 Multiplexer

C(1)	C(0)	Y
0	0	A(0)
0	1	A(1)
1	0	A(2)
1	1	A(3)

Figure (2): (b) Truth Table of 4:1 Multiplexer

3. DIFFERENT LOGIC STYLES

Logic style can be defined as how transistors are used to realize logic function. Speed, size, power dissipation and wiring complication are the features which rely on which logic style is used and they are vary noticeably from one logic style to other logic styles and therefore, for circuit concert selection of appropriate logic style is very helpful. Complementary MOS, GDI, FINFET and LEAP four techniques are used in this paper.

3.1 Complementary MOS Logic Style

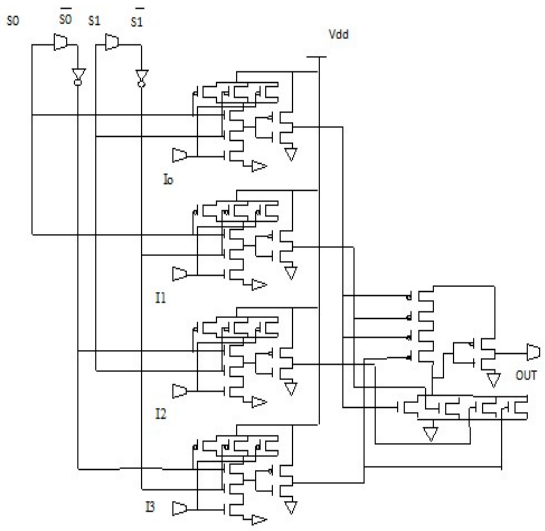

Figure (3): Conventional CMOS base 4:1 Multiplexer

Both NMOS and PMOS transistors are used in CMOS logic style to design logic functions. Both p-type and n-type transistors are joined to the identical input, one type of MOSFET will be immediately on when other MOSFET is off, and vice-versa. In CMOS logic gates n-type MOSFETs are sand witched between the lower voltage power supply rail and output and it is used in a pull down network and p-type MOSFETs are used in a pull up network sand witched between the higher voltage rail and the output. Problem of voltage scaling and transistor sizing is not more in CMOS circuits [6-7].

3.2 Gate Diffusion Input (GDI)

A necessary unit of Gate Diffusion Input cell consists of three terminals- N (external diffusion node of NMOS transistor), P (external diffusion node of PMOS), G (common gate input to both PMOS and NMOS transistors). On the basis of circuit structure and its mode of operation P, D and N can be used as either inputs or outputs. The GDI cell consists of only two transistors PMOS and NMOS for implementation of extensive variety of logic circuits. This technique is most appropriate for the design of fast low power circuits, used to reduce the transistor count by using less number of transistors [8].

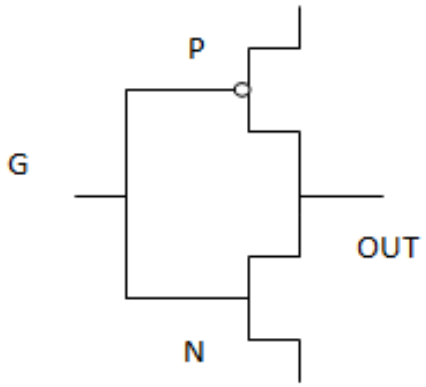

Figure 4: Basic cell of GDI

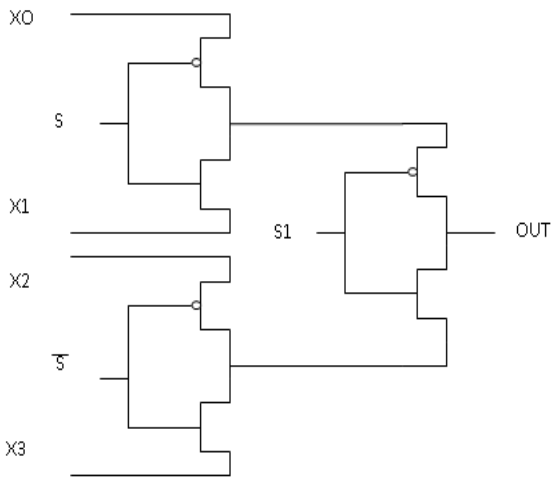

Figure 5: GDI base 4:1 Multiplexer

3.3 FINFET

FINFET, Two transistor of same kind connected with their source terminal and drain terminal attached together which is called double-gate field effect transistor. Usually single-gate field effect transistor is not flexible as FINFET because its two gates controlled separately.

To improve performance and decrease leakage power of transistor second gate of FINFET transistor is used which manage the threshold voltage of the first gate dynamicall[9].

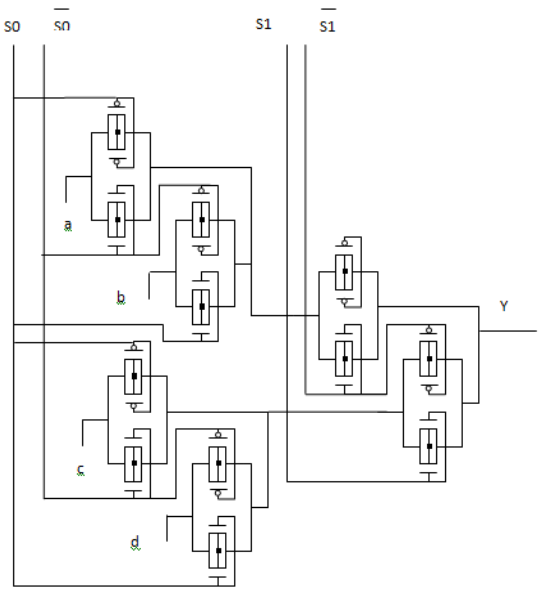

Figure (6): FINFET base 4:1 Multiplexer

3.4 LEAP

LEAP actually stands for lean pass-transistor logic; the reason for that it is called lean. It is thinner, because single-rail logic is used in contrast to dual-rail logic that is used for other pass-transistor members, logic family members. Buffer as it is shown is nothing but an inverter and a weak PMOS transistor for swing restoration. So, this path performs the dual-rail of providing buffer as well as swing restoration logic [10].

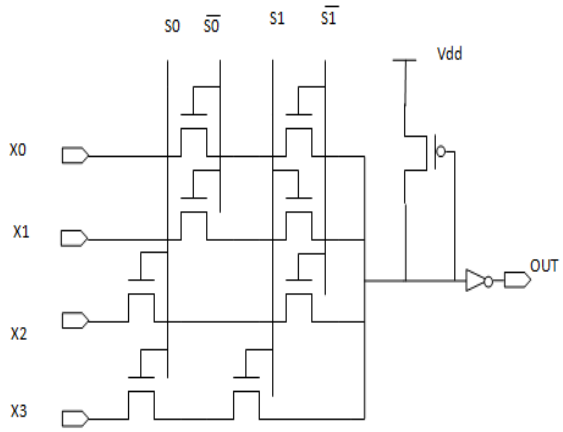

Figure 7: LEAP base 4:1 Multiplexer

IV. SIMULATION RESULTS

In this section, output waveforms of CMOS, Gate Diffusion Input, FINFET logic and LEAP logic are showed and results of these circuits are also calculated.

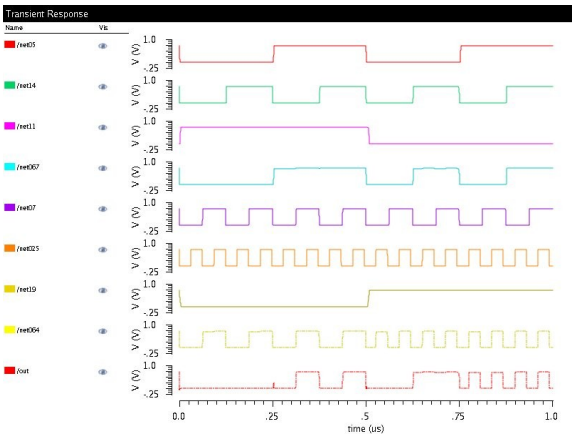

Figure 8: CMOS Waveform

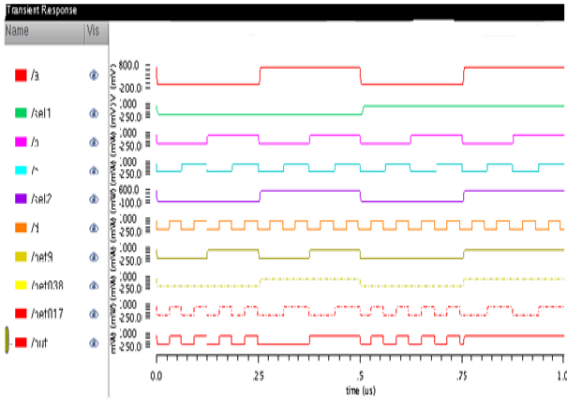

Figure 9: GDI Waveform

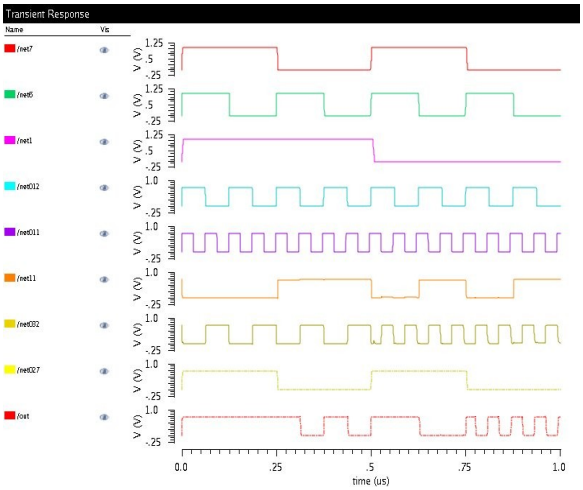

Figure 10: FINFET Waveform

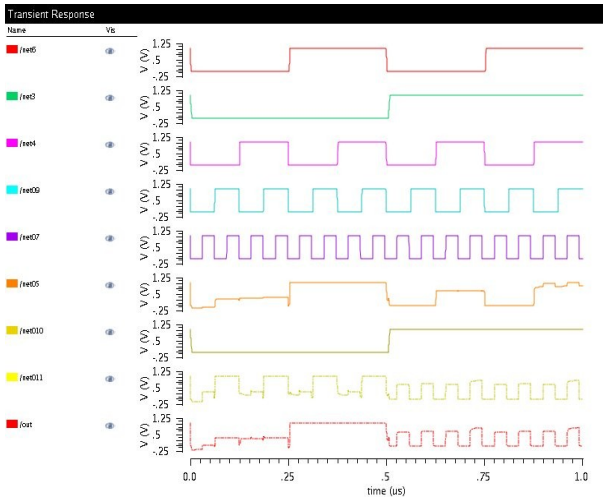

Figure 11: LEAP Waveform

These figures shows that output waveforms of 4:1mux using various techniques

Like CMOS, Gate Diffusion Input, FINFET and LEAP techniques. Four inputs are selected by two select lines and one input goes to output. Three 2:1 mux are used to realize 4:1 mux.

4.1 Power dissipation

Power dissipation mechanism is classified into two classes:

A. Static power dissipation and Dynamic power dissipation

- During active state of circuit Dynamic power dissipation occurs, i.e. some work perform on data.
- due to load capacitances charging and discharging
- When both PMOS and NMOS are moderately on

B. Static power dissipation occurs during off state of circuit or in a power-down mode.

- Sub threshold transmission through down mode transistors.
- Tunnelling current passes gate oxide
- Leakage current in reverse-biased diodes

Ptotal= Pstatic + Pdynamic …….. (1)

Pdynamic=1/2 (CL*VDD2 *fc)……(2)

Pstatic = Ioff* VDD……..(3)

Where,

CL= load capacitance

VDD=Power supply

fc= Clock frequency

Ioff =leakage current drawn by each switch in off state

4.2 Speed

Speed of digital circuits can be found by : Delay

td= (CL * VDD) /Ion……..(4)

Maximum clock frequency:

fc, max= 1/(td * Ld)……...(5)

Where,

CL= load capacitance

VDD=Power supply

Ion= leakage current drawn by each switch in on state

Ld= logic depth (no of stages through which a switching event must propagate during one clock cycle)

4.3 Transistor Count:

Transistor count can be defined as number of transistors is used in device. Transistor count is the most frequent measure of integrated circuit size.

V. COMPRESSION RESULTS

Tech-nique used	Transistor count	Power consump-tion	Delay
con-ventio nal	36	75.596u W	0.588ns
GDI	6	1.875pW	0.032ns
LEAP	13	42.348n W	0.068ns
FIN-FET	24	85.747n W	0.102ns

VI. CONCLUSION

In this paper, the digital circuit 4:1 mux was implemented by different low power techniques namely CMOS, GDI, FINFET, and LEAP. The results were simulated using cadence and comparison has been done for different parameters like power dissipation, delay and transistor count. The results concluded that as compared to other proposed techniques, CMOS has more power dissipation and transistor count. These advantages of proposed techniques over CMOS make them more efficient and convenient to be used in digital circuits.

VII. ACKNOWLEDGEMENT

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