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Performance Analysis of Different Low Power Consumption Full Adders

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ABSTRACT

Full adders being basic structure block of digital signal processors and application precise integrated circuits remains an important area of research over years. All of the devices uses very fundamental arithmetic operation addition of two binary numbers. Full adders may also be designed with the assistance of various logic designs. Different logic styles favors different performance parameters. In this paper performance of 5dissimilar 1-bit full adder cells of different logic styles that is I.) 14T full adder, II.)9b full adder, III.)13a full adder IV.) SERF full adder V.) GDI 10T full adder are equated and evaluated.

All the adders are analyzed and compared on the basis of following parameters:

Comparison of full adders on the base of average power and delay at 0.7V supply voltage.

1. *Comparison of full adders on the base of leakages power at 0.7V supply voltage.*
2. *Cadence VIRTUOSO tool has been utilized for making schematics on 45 nm technology.*

Keywords:— *CMOS, Full Adder, Average Power, Transistor Count.*

I. INTRODUCTION

Electronics is dominating the world in every aspect. The devices size is reducing day by day. This extreme and fast reduction of size of devices has become possible cause of the extensive progress of the semiconductor industry. VLSI plays very vital role in the swift progress of semi conductors. It is cause of the growth of VLSI that we are capable to think about lots of transistors at a single chip. The need and trend of designing ever more compact devices has motivated researchers to work in direction of smaller silicon chip area, high speed, and better battery life. The progress in CMOS technology has made size of chip shrinking day by day. It has lead VLSI industry towards the very big integration density and method on chip designs beyond some GHz operating frequencies[5]. Any electronic device popularity depends on its size, battery life, reliability. In sequence to enhance these desired characteristics we necessity to work on silicon chip size. The extremely crucial parameter which will have to be regarded at the similar time designing any device is the power dissipation.

VLSI (very large-scale integration) works on both digital and analog. In Digital applications, the scaling of the gate delay and

power dissipation is of interest. We can say that the speed of digital circuits can potentially increase by scaling [1]. Investigation efforts in the region of small power VLSI systems have enhanced several folds due to exponential progress of portable electronics devices. With the enhanced in no. of transistors on chip, power consumption of VLSI systems is also establishment that further, join to run time failures and credibility difficulties. Packaging and costly with exorbitant power consumption and cooling procedures become more difficult. Less power consumption is and significant design criteria for IC designers at each phase of design together with delay and region opinion [2].

2. FULL ADDER

Each electronic devices involves of DSP (Digital Signal Processors) and ASIC (Application Specific Integrated Circuits) and Microprocessors. All of the above mentioned devices uses very fundamental arithmetic operation i.e. addition of two binary numbers [3].Binary adders are crucial structure blocks in VLSI circuits and its very needed to do efficient implementation of adders as performance of adders affects the perform of entire system. Operation of full adder can be stated as follow:

Sum = (A xor B) xor Cin
Carry = A and B + Cin (A xor B)

Where, the three 1 bit I/P A, B and Cin are operated to compute the desired two1 bit O/P Carry and Sum.

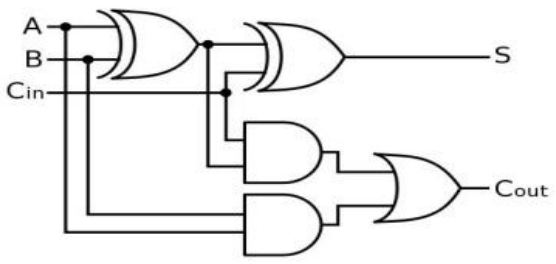

Fig.1. Block diagram of Full Adder Cell Using Gates

Table 1: Truth Table for Full Adder

Input			Output	
A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full adders can be designed exploiting dissimilar logic styles each having their merits and bottle-necks. The dissimilar logic styles that are used to design the full adder affects the size, speed, power dissipation and complexity of any circuit we are designing. As dissimilar logic styles have dissimilar number of transistors exploited, transistor sizes (i.e., channel widths) differ and all these factors determine the overall circuit delay [4].

Full adder can be classified into two sets according to their logic style. One set contain of CPL, TGA, TFA, Hybrid, 14T and 16T and C-CMOS these adders have full swing O/P. These have nice driving capability, high no. of transistors, large areas and mostly power consumption is high.

The other group consists of full adders like Second groups 20T, 9b, 13a, SERF and GDI 10T which do not have swing outputs. The adders of this set have less no. of transistors, 9bdependsfull adder circuit. As no. of transistor is less so area consumed is also less and power consumption is also very less.

In this paper different type of full adders are taken for the analysis. 5 versatile types of adders that is I.) 14T full adder, II.) 9b full adder III.) 13a full adder, IV.) SERF full adder V.) GDI 10T full adder. These 5 adders are already better performers than the conventional full adders. The transistor count is already less for all 5 of them. Adder 13a, 9b, SERF and GDI 10T consist same no. of transistors i.e., 10 but there performance varies from each other due to several factors and different circuit arrangement.

Thus we can say that this paper aims at studying the work that has been done so far in the respective field. One thing to note is all the approaches (different logic style) developed and used by researchers aims to reduce the power dissipation delay and hence figure of merit PDP.

Cadence VIRTUOSO tool has been used for making schematics on 45nm BSIM3 is used for carrying out simulations. Performance of adders are compered on the basis of Average Power, Average Delay, Leakage Power.

III. Analysis Different Type of Adders

14T Full Adder

It is a one of the most efficient adders used these days.14T full adder as shown in fig.3.It has been found during evaluation it tick marks all the boxes of speed, power consumption, delay, etc. In terms of simplicity it less complex than that of conventional adder. It also consumes lesser power than conventional full adder, less delay. Ideally it is a better than conventional 28T Full adder in terms of power consumption, delay, leakage power and also chip size is reduced due to reduction in transistor count. It has 4 transistors XOR that are inverted in the next phase to generate XNOR. These XNOR and XOR are utilized instantaneously to produce Cout and Sum [10].

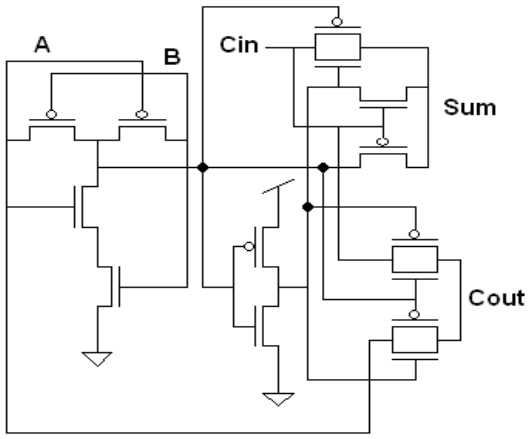

Figure 2. 14 Transistor Full Adder

9b Full adder

It is a 10T full adder. It is first among other 10T adders that are discussed in this paper. All the 10T adders 13a, SERF, GDI 10T including 9b full adder were designed to reduce the power consumption, delay and enhance overall performance of the circuit.

It circuit as shown in fig.4 is simpler than that of other adders. It employs 4 transistor XNOR gate to give the Sum and the Cout is carried out by simply multiplexing two of the inputs i.e., B and Cin which is controlled by (A XNOR B) it is done in the other circuits as well [10].

9b full adder is proven to be a better alternative for conventional full adders that consist large no. of transistors. In terms of performance it shows less power consumption than 14T, 13A, SERF full adder. [11]

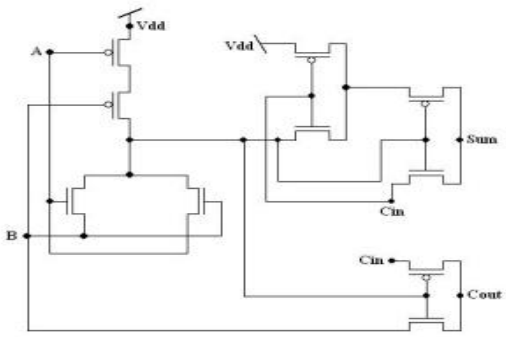

Figure 3. 9b Full Adder

13a Adder

It another kind of full adder that employs 10 transistors to carry out function of full adder. Figure 4 shows the transistor level implementation of 13a adder. 9b and 13a full adder are found more efficient than SERF adder, in terms of power consumption [11].

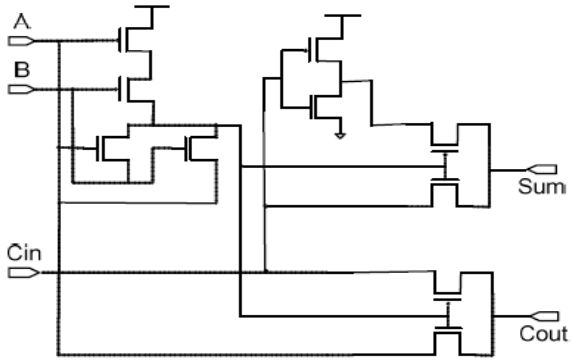

Figure 4. 13A Full Adder

SERF Adder circuit

The static energy recovery full (SERF) adder is illustrate in fig.6, that implements a full adder prepared using only 10 transistors as specified in figure 5. SERF has been shown to consume less power than many other adders. Here the transistor count is not only responsible for the its less power consumption instead elimination of direct contact of ground is the reason behind its performance[10][11]. This circuit is slower than many other adders [10].

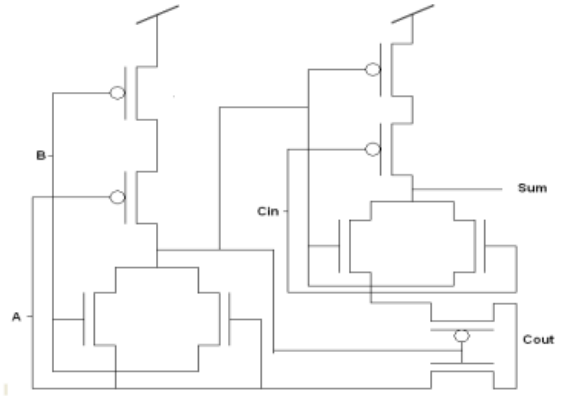

Figure 5. SERF Full Adder

GDI 10T Full Adder

A GDI(Gate Diffusion Input) based 10T full adder is shown in figure 6. Evaluation and observation shows that GDI is very efficient technique which allow realization of versatile logic functions by simply using 2 transistors based circuit.[12] The GDI based 10T adder is very well designed to produce the output with reduced power consumption and transistor count. The addition is carried in the similar way as is SERF adder.

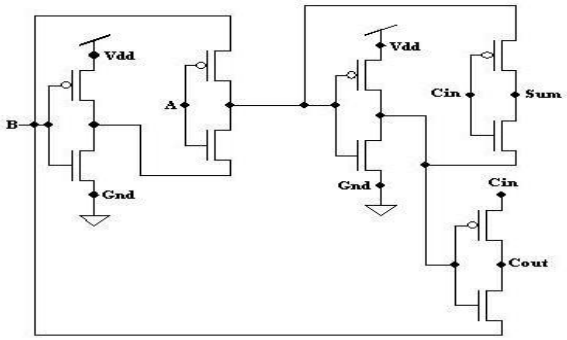

Figure 7. GDI 10T Full Adder

IV. Result And Simulation

The simulation of 14T full adder employing complementary pass logic, 13a, SERF, GDI 10T and 9b full adder cells exploiting dissimilar logic is obtained and compared. The simulation are performed exploiting Cadence Virtuoso which works at 45 nm. The circuits are compared on the base of average power, delay and leakage power of all the full adders configurations.

Table 2. Comparison Results Between Different Full Adder cells

Name of Full Adder	Average Power	Delay	Leakage Power
14T	302×10^{-9}	8.56×10^{-9}	61.43×10^{-12}
13a Adder	51.258×10^{-9}	40.43×10^{-9}	44.82×10^{-12}
SERF Adder	125.8×10^{-9}	15.1×10^{-9}	28.90×10^{-12}
GDI 10T Adder	31.70×10^{-9}	24.15×10^{-9}	7.498×10^{-12}
9b Adder	84.98×10^{-9}	16.33×10^{-9}	38.6×10^{-12}

Also the input output waveforms of 14T Full adder, 13a, 9b, SERF and GDI 10T full adder carried out after simulations are shown below:-

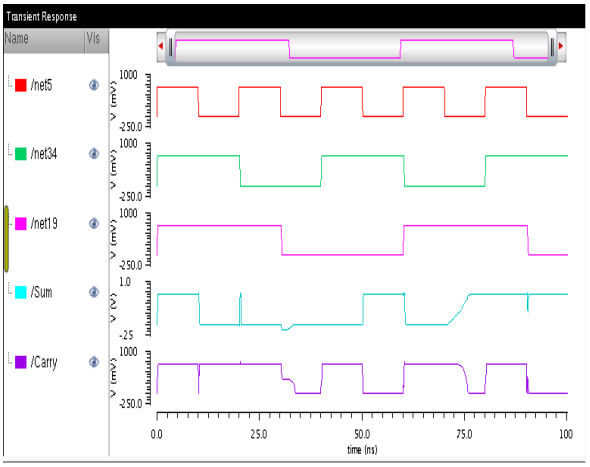

Figure 8. 14T Waveform

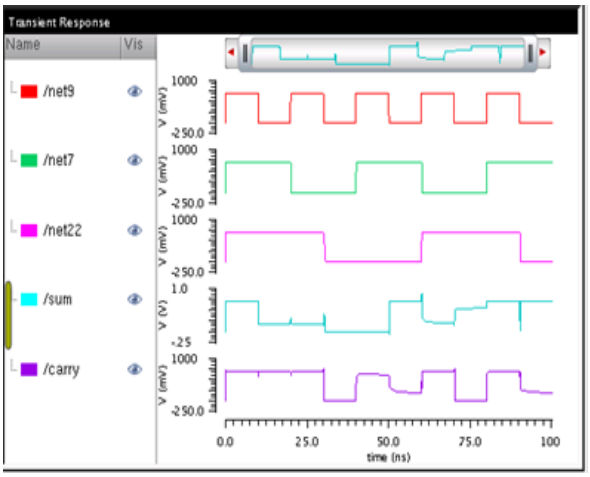

Figure 8. 9b Waveform

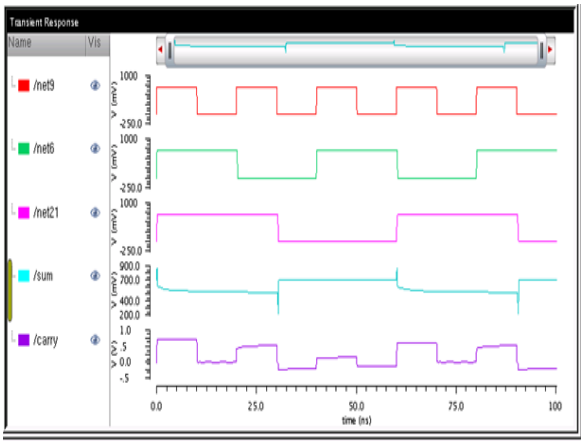

Figure 10. 13a Waveform

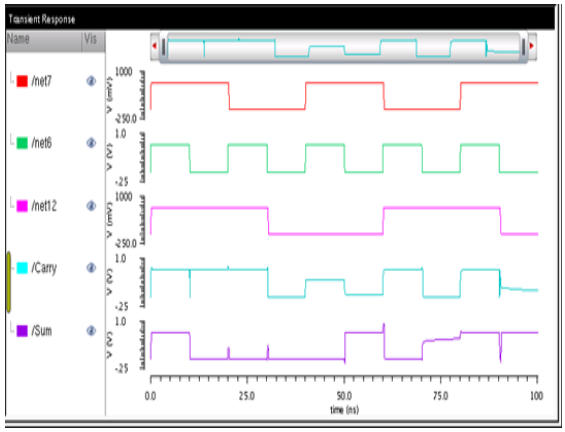

Figure 11. SERF Waveform

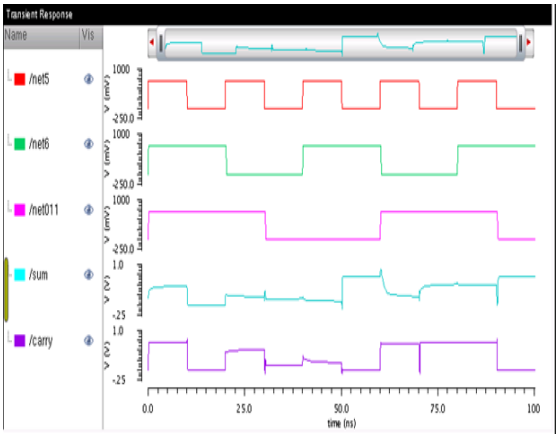

Figure 12. GDI 10T Waveform

V. CONCLUSION

In the present paper six circuits of full adders are presented. All the full adders employing different logic style. The simulation results of full adder at 45nm technology shows that the SERF full adder shows very good performance in terms of average delay with supply voltage of 0.7V. Power Dissipation of GDI 10T full adder is efficient comparison to the another full adder cells, which is very less than in compares to another full adder cells having same supply voltage of 0.7V. GDI 10T full adder also has very less leakage power in comparison to other. But using GDI is costly affair. As I said earlier also every design has their merits and bottle necks we cannot say that one is perfect. Some cells consumes less power but have more delay and vice versa.

To resolve such issues researchers have found a smart way to resolve such issues these days Hybrid style of full adder is used these days. As Hybrid design comprises two or more than type of full adders so they sort the purpose with each full adder being compatible with each other. Hybrid designs are the future and smart way to fulfill desired requirements.

VI. ACKNOWLEDGEMENT

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REFERENCES:

[1] Behzadrazavi, (2001) "Design of Analog CMOS Integrated Circuits", Newyork: McGraw-Hill, 2nd edition.

[2] Manoj Kumar, Sandeep K Arya & Sujata Pandey, "A New Low Power Single Bit Full Adder Design with 14 Transistors Using Novel 3 Transistors XOR Gate", IJMO Trans., Vol. 2, No. 4, August 2012.

[3] Partha Bhattacharyya, Bijoy Kundu, Sovan Ghosh, Vinay Kumar and Anup Dandapat, "Performance Analysis of a Low Power High Speed Hybrid 1-bit Full Adder Circuit", IEEE Trans. on VLSI systems.

[4] Reto Zimmermann and Wolfgang Fichtner, "Low Power Logic Styles: CMOS Versus Pass Transistor Logic", IEEE Journal of Solid State Circuits, Vol. 32, No. 7, July 1997.

[5] Kapil Mangla and Shashank Saxena, "Analysis of Different CMOS Full Adder Circuits Based on Various Parameters for Low Voltage VLSI Design", International Journal of Engineering and Technical Reasearch, Vol. 3, Issue 5, May 2015.

[6] Chyn Wey, Chun-Hua Huang, and Hwang-Chemg Chow "A New Low-Voltage CMOS 1-Bit Full Adder for High Performance Applications", IEEE Trans., 2002.

[7] Farshad Moradi, Dag. T, Wisland, Hamid Mahmoodi, Snorre Aunet, Tuan Vu Coal & Ali Peiravi, "Ultra Low Power Full Adder Topologies", IEEE Trans., December 2009.

[8] Nima Taherinejad and Adib Abrishamifar, "A New High Speed, Low Power Adder; Using Hybrid Analog-Digital Circuits", IEEE Trans., 2009.

[9] Anjali Sharma and Rajesh Mehra, "Area and Power Efficient CMOS Adder Design by Hybridizing PTL and GDI Technique", IJCA Trans., vol. 66- No.4, March 2013, pp. 0975-8887.

[10] Saradindu Panda, A. Banerjee, B. Maji, Dr. A.K. Mukhopadhyay, "Power and Delay Comparison in Between Different Types Of Full Adder Circuits", IJAREEIE, Vol. 1, Issue 3, September 2012.

[11] Ankita Gupta, Rajeev Thakur, "A Survey On Different CMOS Full Adder Design Technique", IJARCSSE, Vol.5, Issue 7, July 2015.

[12] Dornam Teja Ravindar, V. Venkanna, "Design & Study of a Low Power High Speed 10T Full Adder Using GDI Technique", IJMETMR, Vol.3, Issue 9, September 2016.

[13] M. Morris Mano, "Digital Design" – Third Edition, Prentice Hall of India private limited, 2006

[14] N. H. E. Weste, and K. Eshraghain, "Principle of CMOS VLSI Design, A System Perspective," Pearson Education, 2010.

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