Volume 4, Issue 3, July 2017 ISSN: 2348-8565 (Online)
International Journal of Modern Engineering and Research Technology
Website: http://www.ijmert.org Email: editor.ijmert@gmail.com

Modeling and Optimization of Low Power Memristor based Non-volatile 7T SRAM Cell

Daya Ram Yadav
Research Scholar M. Tech.
Mewar University
Gangrar Chittorgarh (Rajasthan), [INDIA]
Email: dryadavdig@gmail.com

D. C. Chaurasia
Director
Pandit Dev Prabhakar Shastri College of Technology
(PDPSCT) Chhatarpur (M.P.), [INDIA]
Email: mapdc3046raj@yahoo.co.in

ABSTRACT

The semiconductor memory device of the most important subsystems of modern digital systems. The expansion of the new era of silicon technology stores the memory of the results quickly, many information can be obtained to continue to produce a large memory chip. However, the energy consumption rate of the increase is reduced due to the high density. Therefore, for a low power consumption plan, there is a need for high speed storage. Objectives while maintaining competitiveness, but need to reduce the capacity of the cache memory array. Several current technologies and a brief description of their strengths and weaknesses. Power reduction technology helps to reduce energy leakage SRAM circuit back into the active range. SRAM design and a simple calculation, based on parameters Memristor SRAM, which is based on the SRAM MTCMOS Memristor: Memristor SRAM, which is used to design and compare the results to conventional SRAM: design and calculation of the film is usually SRAM standards-based cadence tool of 45 Nanotechnology with operating voltage is 0.7.

***Keywords*::—** *7T SRAM (CMOS), 5T SRAM (MEM), Memristor, Parameters, Implementation.*

I. INTRODUCTION

In the future, mobile phone, notebook, computer, PDA, tools, the demand for mobile devices such as electronic computer area is growing. Low-power electronic system is added, the system uses memory to store data. The type SRAM: When the device is connected to the power of the SRAM data source transistor from the light loss other means of information technology, such as volatile SRAM specifications, and it is not necessary to operate the system characteristics of memory chips (memory, between the alignment processor SOC reduction Latency). The advantages of SRAM because it is used to develop portable systems, low-power SRAM is so serious mobile devices based on this file Memristor SRAM: This article is designed for 7T SRAM purpose. Memristor uses low-power SRAM to develop. Memristor the two ends of the linear variable resistor, known by the electrical element, as a feedback. Electrical load with the flow channel in a certain time interval. It depends on the size and polarity of the voltage up Memristor resistance. It has a nonlinear relationship between voltage and current storage device. Simple membrane technology, power consumption and power loss SRAM is generally reduced.

II. 7T SRAM Cell Operation

7T SRAM dependent concept both investors and the feedback unit before the recording process. Feedback and the distance are achieved by the NMOS transistor. BLB cells depend on for write operations. The operation of the recording shall be close to the reverse connection. Send a BLB additional input data. SRAM cell, two inverters are connected in series. Before the development of BL and BLB, these energies, such as INV2. Internal switch actuators, after each read / write "high" pre-load INV1 send entry summary data.

If the "0", BSB ignores the energy consumption of "high". Write "0" in comparison to the consumption of paper energy, "1", BLB reset scheme, the result of an activity coefficient of each recording process, and the bit line BLB set as "1" to do.

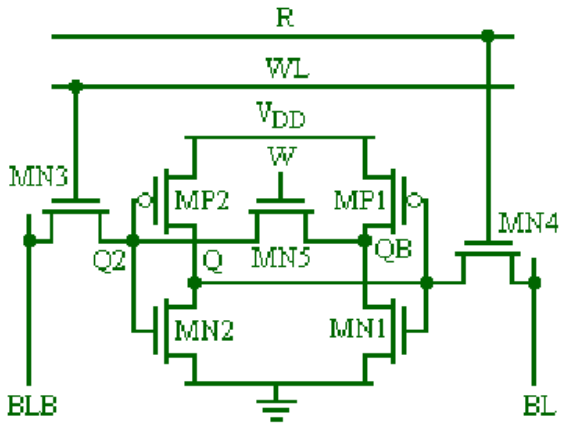

Figure 1. Circuit Diagram of 7t SRAM Cell Operation

III. Read Operation

During a read operation, the word line controller is disconnected outside the word line is activated. The inverter in the SRAM cell, since the correction bit of the logic, it can determine this value. Pre-charge exhaust gas immediately after the previous step, which is a read mode and write operations. In read mode and loads the internal node and a stable record SRAM7T: If the feeder is not the case (interfering signal limit is too small) is strong enough, it can not be removed from the stored value of certain bit line load encrypted.

IV. Write Operation

To process, it is necessary to switch to a three-phase driver, the bit line is increased. You can easily stabbing around in pairs. Internal audit is due to the fact that it is much smaller than the external controller. Therefore, the data axis division includes nanoseconds selection word line transistor. Data recording device is applied to the bit line. The transistor, which is available through the authorization of the word line WL, signal port "1". The data "0" is stored in the memory storage unit to "1" when the current decreases to a storage device on the storage node corresponding bit high output, "0" is equal to the applied voltage. Voltage storage node to the other inverter fault is less than the contents of the backward movement of the unit. Voltage "0" and "1" storage node when it should be included in the reverse order. If retains first place in "0", then data bit line, if "0" does not change the condition of the battery. A bit of string and stores in the storage unit, "1" and data "1" when there is no change in the cell.

V. MEMRISTOR

Memristor traffic passive elements are arranged in accordance with the size and polarity of the voltage resistor. With non-linear relationship between the voltage of the memory device.

Figure 2. MEMRISTOR

It gives relation between flux Φm and charge (q). Defined as two non-volatile communication device, the size of the flow of the computing power measures and has been designated M, such as charges Q. mathematical expression:

$$M(q) = \frac{d\Psi m}{dq}$$

Where M is the Memristor, Φm is the magnetic flux and q is the charge.

VI. MEMRISTOR BASED SRAM

SRAM well known results, but this kind of memory and memory problem makes it unstable. New techniques to overcome these problems is to reduce the energy consumption, increase the speed of the read / write. In this study, based on advanced SRAM Memristor. In this way, as is the case, simple SRAM historical data and the memory is cleared, leaving enough time for the system based on the properties of memristor in the non-volatile memory SRAM. In fact, a variable power supply based on external factors memristor no movie to stored when they are disconnected. According to the data holding circuit, there is a power source to hold this state is not required.

Barrier in contact with the two memory devices, transistors, except that it consists of a three-terminal device, such as a switching transistor of Memristor. It consisting of two thin layers, the layers are arranged between the nanometer and the nanowire layer. Doping and undoped titanium dioxide, from a layer of titanium dioxide. The layer of titanium dioxide, is the resistance change of two layers of layers of absorption of oxygen ions and oxygen ions, other losses of them. Ion charging movement, which is the base layer of titanium dioxide, changes Memristor resistance movement. In other words, a variable resistor, which is why the use of memories. Therefore, Memristor can reduce the total capacity of SRAM-based memristor.

VII. POWER DISSIPATION

The energy consumption is derived from two educational programs Static and dynamic power consumption

- Dynamic power circuitry when some data creation task is active.
- Since the capacities of a load-lifting
- PMOS and when suitable and effective NMOS
- Circuit is in off state or in the static power dissipation mode occurs, the static power consumption.
- Transistor auxiliary transfer mode with low threshold electrode
- Tunnel current through the gate oxide film
- Reverse bias diode leakage current

$$Ptotal = Pstatic + Pdynamic$$

$$Pdynamic = \frac{1}{2}(CL * VDD2 * fc)$$

$$Pstatic = Ioff * VDD$$

Where,
CL= load capacitance
VDD=Power supply
fc= Clock frequency
Ioff =leakage current drawn by each switch in off state

VIII. LEAK CURRENT ANALYSIS

The memory will be the bits in the grid matrix. Most importantly, it is a small escape from the cell functions.

- This analysis shows low thermal disposal of batteries.
- The main plot of this test - you can see the size of the field
- A long column read operation (VNK unselected).
- Milf registration along a guide is necessary to have a construction Physical memory.
- Leakage current are analyzed to the same bit cell using q is initialized to Vdd.

- ˜q is initialized to 0.
- WL is OFF and therefore is set to 0. b and ˜ bis at P recharged.
- The leakage current is measured as current through M3 (gateway NMOS transmissions for data 0).
- What happens when the leakage current is high. In this case, when we try to read the value.
- After a little memory, we can read the current value.
- Other non-selected cell leakage current through the ground enough.
- Therefore BT and BB lines, there is no better product value.
- Here, we have a technology for analysis of 45 nm.
- Vdd is 1.1v.
- Vss is 0v.

IX. Speed

High-speed digital circuits can be found: delay

$$td = \frac{(CL * VDD)}{Ion}$$

Maximum clock frequency:

$$fc\ max = \frac{1}{td * Ld}$$

Where, CL= load capacitance
VDD=Power supply
Ion= Current leakage, drawn by each of the included states
Ld= logic depth (no of stages through which a switching events through the clock cycle)

X. Leakage Reduction Techniques

The new technology reduces leakage to other people, and the requirements of the system can be optimized to streamline the program a series of changes to the development, production technology to reduce, supported up / implementation when there is a need to provide technical assistance runtime Develop (Dynamic). There is a variety of methods that planning is described in this section of the drain described to reduce SRAM to remove static power consumption cell.

Table 1. Comparison of 7t SRAM and 7t Memristor Based SRAM

	7T SRAM (CMOS)	7 T S R A M (MEMRISTOR)
Power	2.439E-6	5.96E-6
Leakage Current	625.9E-15	97.02E-12
Leakage Voltage	113.2E-3	212.8E-3

XI. Advantages of CMOS Technology

In most cases, it is achieved by an SRAM cell, which has the advantage of such low static power consumption. However, when the current reading operation such as potential "0" is achieved in the problem of the “1”, “0” coating NMOS whose voltage power unit is stored. In addition, positive feedback mechanism is increased to “1”. In addition to the node.

- Production capacity
- Good margin of noise immunity
- Figured (in hazardous conditions, work reliably)
- Lower switching activity

XII. Disadvantages

- It takes a lot of transistors
- Weak output processing
- Short-circuit power
- power dissipation

XII. Conclusion

The proposed memory was developed with the rhythm CMOS / VLSI technology 45nm. The software used in the project, we will design, simulation can be integrated with the physical description of the circuit. The proposed project is designed 7T-SRAM-based Memristor. It is not a transient nature of Memristor. Pack density increases, the system chip (SOC) decreases, these techniques reduce data stored

without power supply with reduced leakage current device. SRAM is that we have the ability to develop SRAM-based speed in this way, make-up most of the performance to the area.

REFERENCES:

[1] Vijay Singh Baghel and Shyam Akashe, "Low Power Memristor Based 7T SRAM Using MTCMOS Technique," 2015 Fifth International Conference on Advanced Computing & Communication Technologies in MP, India.

[2] Thangamani. V, "Memristor-Based Resistive Random Access Memory: Hybrid Architecture for Low Power Compact Memory Design," Control Theory and Informatics ISSN 2224-5774 (Paper) ISSN 2225-0492 (Online) Vol.4, No.7, 2014.

[3] Design of 7T SRAM Cell for low power appliances, "India Conference (INDICON), 2015 Annual IEEE" 10.1109/INDICON.2015.7443657

[4] Jörg Schulze: *Concepts of Silicon-Based MOS Components*. Springer, Berlin, 2005, ISBN 3-540-23437-3, pp. 66-67, 297-314.

[5] Farshad Moradi and Jens K. Madsen, "Robust Sub threshold 7T-SRAM Cell for Low-Power Applications," 978-1-4799-4132-2/14/$31.00 ©2014 IEEE.

[6] Artificial synapses could lead to advanced computer memory and machines that mimic biological brains, HRL Laboratories, March 23, 2012, retrieved March 30, 2012.

[7] G.-F. Wang, W. Kang, Y.-Q. Cheng, J. Nan, J.-O. Klein, Y.-G. Zhang, and W.-S. Zhao, "Low Power Computing Paradigms Based on Emerging Non-Volatile Nanodevices," Journal of Electronic Science and Technology, Vol. 12, No. 2, June 2014.

[8] Amit Grover, "Low Power 7-T SRAM using 90 NM Technology with Tanner Tool," 2013 First International Conference on Artificial Intelligence, Modelling & Simulation.

[9] U. Supriy, K. Ramana Rao, "Design of Low Power CMOS Circuits using Leakage Control Transistor and Multi -Threshold CMOS Techniques," IJCTA, July-August 2012.

[10] Meuffels, P.; Schroeder, H. (2011), "Comment on "Exponential ionic drift: fast switching and low volatility of thin-film memristors" by D.B. Strukov and R.S. Williams in Appl. Phys. A (2009) 94: 515-519", Applied Physics A, **105**: 65–67, Bibcode:2011ApPhA.105...65M, doi:10.1007/s00339-011-6578-7

* * * * *