



VLSI Implementation of Carry Select Adder Using Verilog

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ABSTRACT

The Carry select adder (CSLA) is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input, then the final sum and carry are selected by the multiplexers (mux). The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA to achieve high speed and low power consumption. In digital system, mostly adders lie in the crucial paths that affect the whole performance of the system. Experimental analysis illustrates that the proposed architecture achieves advantages in terms of speed, area consumption and power.

Keywords:— Carry Select Adder, adder, mux, VLSI, BEC

I. INTRODUCTION

Outline of area and power effective rapid information rationale frameworks are a standout amongst the most considerable areas of exploration in VLSI framework plan. In gadgets applications adders are most generally utilized. In computerized adders, the speed of expansion is restricted when needed to

engender a carry through the snake. The aggregate for every bit position in a elementary adder is produced consecutively strictly when the past bit position are summed and carry spread into the following position [1].

The CSLA is utilized as a part of numerous computational frameworks to allay the issue of carry spread postpone by free era different conveys and afterward select a carry to create the aggregate. On the other hand, the CSLA is not an area productive on the grounds that it utilizes different sets of Ripple Carry Adders (RCA) to produce halfway total and carry by considering carry include as $C_{in}=0$ and $C_{in}=1$, then the last summation and carry are chosen by the multiplexers. The Carry select adders are delegated Linear Carry select adders and Square-root carry select adders [2]. The fundamental square-root Carry Select adders has a double ripple carry adder with 2:1 multiplexer, the principle detriment of consistent CSLA is the expansive area because of the different sets of ripple carry adder.

In this paper, modified CSLA using BEC has introduced to reduce area and power consumption with slight increase in delay. The basic idea of the proposed architecture is that which replaces the BEC by common Boolean logic with enable signal[9]. The proposed architecture reduces the area, delay and power. [10] This paper is organized as follows; section 2 review the related works and section 3

Table 1. The Truth Table of Single Bit FA and Single-bit Full-Adder with Modified BEC

C_{in}	A	B	S_0	C_0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

3.1 Modified CSLA Architecture

This method replaces the BEC add one circuit by Common Boolean Logic. The output of full adder waveform for carry in signal is '1' and it generates the carry signal and summation by just using an OR gate and INV [18]. It is shown in figure 2.

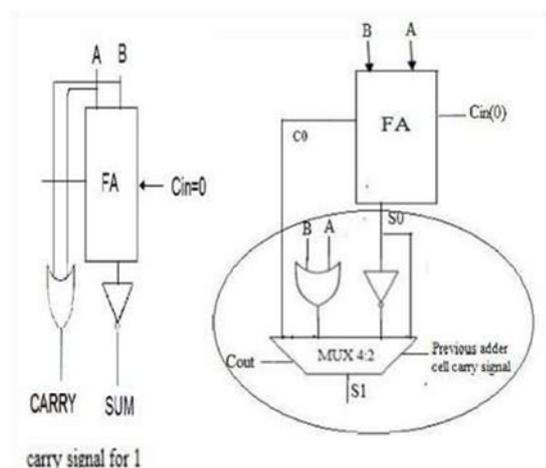


Figure 2: 16-bit SQRT CSLA using Modified BEC

The carry signal and summation for FA which has $C_{in}=1$, it is generated by the INV and OR gate. With the help of multiplexer, we can predict the correct output result according to the logic state of each carry-in signal. Internal structure of the group 3 of Proposed CSLA is shown Fig 3. A Manual counting of number of

gates is used for group 3 is equal to 36 (full adder, half adder, and multiplexer, not, or gate) [12]. One input to the mux goes from the RCA block with $C_{in}=0$ and other input from the CBL.

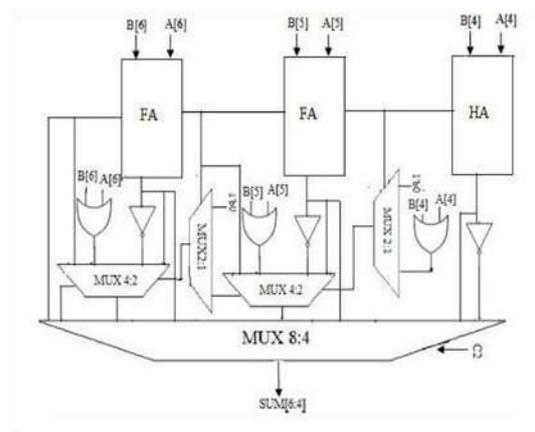


Figure 3: Modified BEC

The Group 3 performed a three bit addition which are A [4] with B [4], A[S] with B[S] and A[6] with B[6]. This is done by 1 half adder (RA) and two full adder (FA). The CBL block has a 4:2 multiplexer to select the appropriate carryout and summation signal for Carry-in signal '1'. Through 2: 1 multiplexer the carry signal is propagate to the next adder cell. The 6:3 multiplexer and 4:2 multiplexer is the combination of 2: 1 multiplexer[14].

IV. PERFORMANCE EVALUATION

The proposed design used in this research work has been developed using synthesized in Cadence RTL compiler using typical libraries of TSMC 0.18 um technology Verilog- HDL. The synthesized Verilog netlist and their respective design constraints file (SDC) are imported to Cadence SoC Encounter and are used to generate automated layout from standard cells and placement and routing. Parasitic extraction is performed using Encounter's Native RC extraction tool and the extracted parasitic RC (SPEF format) is back annotated to Common Timing Engine in Encounter platform for static timing analysis.

The performance of the proposed approach is evaluated using the performance metrics such as Delay, area and power. Several real time implementation strategies were discussed in [15], [16] and [17].

4.1 Timing Analysis

The Timing analysis has been done in ISE simulator the output obtained is shown in figure 6.

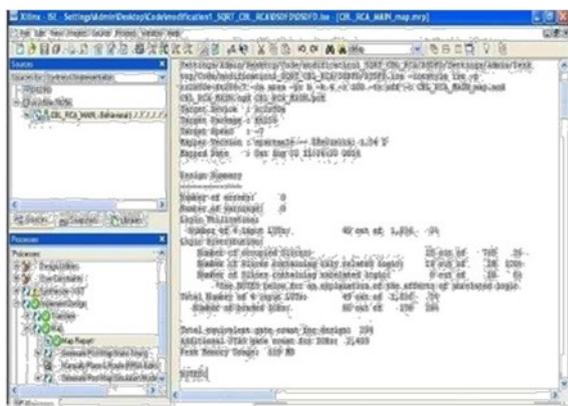


Figure 4: Timing Analysis

4.2 Comparison

In the following given table which target FPGA has been used belongs to Spartan 3 (family), XC3S400 (device), TQ144 (Package), -5 (speed grade).

Table 2. Comparison Table Maximum Combinational Path Delay (in ns) for Different Carry Select Adder at 16 Bit Level

M.N.V. Anusha,	S. Balaprasad	Result
K. Babulu[5]	[3]	Obtained
17.21	27.1	12.10

V. CONCLUSION

In this paper analyzed the logic operations involved in the conventional and BEC-based CSLAs to study the data dependence and to

identify redundant logic operations. And also eliminated all the redundant logic operations of the conventional CSLA and proposed a new logic formulation for the CSLA. The modified SQR CSLA reduces the area and power when compared to regular CSLA with increase in delay by the use of Binary to Excess-1 converter. This paper proposes a scheme which reduces the delay, area consumption and power than regular and modified CSLA by the use of modified BEC. In future work, It would be interesting to test the design of the proposed 128-b SQR CSLA by Quantum dot Cellular Automata (QCA) method. In brief, we propose another adder, that achieves all conditions of competitors and accomplishes the best area-delay tradeoff by using a majority gate. The above preferences are obtained by utilizing an overall area/space to the less expensive plans as known in the literature.

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